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Dynamic and Static Mapping Methods in Two-Dimensional Network on Chips

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Abstract
Network- on- chip **(**NoC**)** architecture has been suggested for fixing problems of system on chip (SoC or SOC) communications. Mapping of cores on a specific substrate is one of the three dimensions in designing network on chips which many algorithms have been suggested by various groups for optimize it. Therefore, in this paper, we have examined the concept of mapping in the network-on-chip and some of the methods used in this dimension of the design, such as genetic algorithm, branch and bound, bee colony, ant colony, clustering and decision tree structure in the two-dimensional substrate. Furthermore, for these algorithms we measured the important parameters in the efficiency, such as power consumption, latency, congestion and communication costs. Finally, we pose some suggestions for future work.

Keywords: Evolutionary Algorithms, Power Consumption, Network -on- Chip **(**NoC**)**, Dynamic Mapping, Communication Cost.

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1. Introduction

Due to the lack of efficiency of the communication buses used in the on- chip System, for the high number of processors, the subject of network -on-chip or NoC has been raised in the early of the current decade. There are three overall axes in designing on-chip network: designing the communication infrastructures, designing the appropriate routing and designing a suitable mapping in order to locate the cores in a right home of the NoC. After designing a communicative infrastructure that includes items such as topology, bandwidth and so on, the appropriate routing design is raised. It should be noted that there is a direct relationship between routing and mapping. A more suitable mapping will be followed by a more suitable routing. As the main focus of this study is on concept of mapping, so, concept of mapping is initially reviewed in brief. Then, since more recently the use of heuristic algorithms for mapping of network-on-chip is very important for solving NP-hard problems, so we will evaluate some of the methods outlined in this aspect and other mapping algorithms that are based on dynamic and static modes.

2. Mapping in NoC

One of the fundamental concepts in the network is the arrangement of the cores in the desired topology. The results of the mapping have a high effect on the energy consumption rate, the average of delay and other parameters of service quality. The importance of this issue is in this that in nanotechnology, decreasing energy consumption is the most important priority in designing, and a suitable mapping can we help in reaching this goal. Therefore, for this purpose, we investigate some of the two - dimensional mapping algorithms:

2.1. CoNA: Dynamic Applied Mapping for Reduction of Congestion on Multi-Core Systems

In the CoNA algorithm, internal and external congestion is reduced. Tests show at least an interest of 40% in different mapping cost functions and also on average a reduction of 16% of network delay in comparison with existing algorithms [1].

2.2. Relative Analysis of Heuristic Dynamic Task Mapping in Heterogeneous NoC-based MPSoCs

On eight heuristics, in terms of response time the applied tasks are compared that this time is between the issuance of a work and when implementation and its communication are completed. By taking the time of waiting, communication and the implementation of the work, the quality of the different heuristics can be evaluated and it is demonstrated that they are recovered [2].

2.3. A Mapping-Based Artificial Bee Colony for Designing NoC with a Specific Application

By awareness of energy in designing NoC, a new mapping algorithm based on the model of an artificial bee colony (ABC) has been proposed for solving the problem of mapping optimization. The result of an optimal mapping is obtained through the transmission of information among the various specifications. A comparison between the proposed algorithm with genetic algorithm (GA) and the mapping algorithm- based ant algorithm system shows that the new algorithm has lower power consumption and faster convergence rates. The results of the simulations of the results show that based on ABC approach, energy can be saved with 15.5% in the MMS, 5.1% in MPEG-4 decoder and 12.9% in VOPD compared with MMAS [3].

2.4. New Heuristic Algorithms for Mapping and Routing of Application with the Knowledge of the Energy in the Mesh -Based NoCs

In [4], a new heuristic algorithm with low complexity, CasNet, for the applied mapping and the routing algorithm with bandwidth bounds for the mesh-based NoC architectures in order to minimize energy consumption have been provided. The provided procedure has been compared with a method that generates optimal solutions, and with two other heuristic algorithms. Tests in the multimedia field show that the proposed mapping algorithm is optimal, or at worst case, obtains about 6% of the optimal solutions in a very short time.

2.5. A New Applied Mapping Strategy for the NoC based on the Mesh of the Tree Structure

In [5], applied mapping problem for No Cbased on the mesh of trees (MOT) structure can be raised. Here a new algorithm based on Kernighan-Lin partitioning is proposed to identify the related cores in applications. Then, using a heuristic algorithm the other nodes are mapped to the topology. In a comparison with the mesh mapping results the results of the MoT mapping have been provided for some usages.

2.6. Applied Mapping Method based on Clustering for NoC

Several heuristic methods have so far been presented. Scalability is the main problem of heuristic methods and in this regard that the heuristic

methods are better than the other methods, decision-making is very hard. Based on these methods, integer linear programming (ILP) specifies the optimal mapping. However, they will need very long execution time. In [6], a relaxation- based clustering is proposed for formulation of the ILP. Experiments conducted on a few multimedia criteria and conventional graphs show that the proposed method obtains the optimal or near optimal results within an acceptable time.

2.7. Applied Mapping on the Structure of the NoC-based Mesh Using Particle Swarm Optimization (PSO)

In [7], a mapping method proposes new application for the NoC-based mesh using PSO. The results for some applications have been compared and provided.

2.8. Low-power NoC Process Element Mapping using a Genetic Algorithm (GA)

Mapping of No process elements is an NP-complete problem, and the results will affect directly on the chip power and other features; so, how to get a mapping solution with low effective power for an issue is a problem faced by the designers of the NoC. Based on the analysis of communication model of NoC, in [8], a target function with power priority and a simulated annealing mapping algorithm are offered. This algorithm combines the ability of the overall calculation of genetic algorithm and local search ability of the annealing algorithm, and also low power mapping solution is accessible using an adaptive crossover parameter, mutation factor, and memory variables. Simulation results show that the rate of convergence of the algorithm has been increased to the 30% to 40% compared to conventional genetic algorithm and has very good effect in the overall optimization.

2.9 NoC -based Mesh Applied Mapping

In [9], a mapping solution and scheduling based on a population-based incremental learning (PBIL) algorithm are offered. Simulation results show that the PBIL approach is able to find the optimal mapping and scheduling in a multiple-target method. A heterogeneous two-dimensional mesh has been used as the target architecture for implementation; furthermore, PBIL is proper to cope with more complex architecture, such as the 3D mesh.

2.10. Simulated Annealing (SA) Optimized Parameter for the Applied Mapping on a NoC

Applied mapping is a critical issue in the design of NoC -based system with many cores. SA often has been applied for searching the optimal solution for the issue of the applied mapping. The parameters applied in SA algorithm control the annealing timing and have a high impact on the run-time and the quality of the final solution of the SA algorithm. Parameters optimized in a regular route for each issue of individual mapping should be selected for all issues rather than using the same set of experimental parameters. In this work, an optimization model, simple Nelder-Mead method is used to obtain the SA optimized parameters. The research shows that SA algorithm, using the optimum parameters, is averagely 237 times faster than what uses the experimental data to set the parameters. For a set of criteria, the SA algorithm with proposed optimized parameters acquire a comparable energy consumption using 1% repetition less than its use in former work [10].

2.11. The Task Mapping- based Tree Model with Knowledge of the Collision in the Multi-Core NoC

Here a tree- model task mapping algorithm is suggested that accepts greatly bandwidth bounds on communicative channels. A quantitative comparison shows that the proposed algorithm, with knowledge of the proposed congestion, considerably reduces bandwidth and balances the workload on the communication channels, while the overhead of weighted communication value is minimized [11].

2.12. Design of Robust Routing Algorithm and Core Mapping in the NoC: an Approach Based on Multi-Target Evolution

In [12], a new method is proposed that corrects simultaneously function of routing and mapping so that Pareto optimal configuration, which optimizes the average communication delay and robust routing, can be determined. The method presented will be used in both scenarios of real and artificial traffic. The results show how the solutions provided through the proposed method in both terms of efficiency and fault tolerance have been possible better than other proposed methods.

2.13. Reliable NoC Mapping Based on Scatter Search

NoC is a promising solution for on-chip systems. Mapping of IP cores on NoC architecture is a major step in the design of NoC. This efficiency highly affects the NoC. In [13], a multi-target optimization algorithm based on scatter search is proposed for NoC mapping. Here evaluation of NoC mapping reliability is mentioned to achieve the NoC architectures with high reliability and efficiency. Experimental results show that this algorithm attains low power consumption, small communication time,

load-balanced links and high reliability compared to traditional evolutionary algorithms.

2.14. A Scatter Multi-Target Search Algorithm for Optimization of NoC Mapping with Error Tolerance

IP core mapping to a NoC is a main step in the design of NoC and affects the efficiency of NoC systems. In [14], a mapping optimization algorithm and a mechanism with the error tolerance have been suggested. The error tolerance mechanism and the corresponding routing algorithm are able to receive the NoC communication from switch faults, while retaining a high efficiency. The mapping optimization algorithm is based on the scatter search (SS), which is a smart algorithm with powerful combined search capabilities. In order to match with the needs of the application of NoC mapping, the SS standard is improved for optimization of multiple objectives. This method helps to obtain the initial designs of mapping with high efficiency. The proposed algorithms are run on the combined criteria sequence of embedded systems (E3S). The experimental results show that the optimization algorithm with low energy consumption and low communication time obtains a moderate link load in comparison with genetic algorithm and PSO.

2.15. Applied Mapping on a MoT Structure based on the NoCusing Discrete PSO

In [15], the issue of applied mapping was investigated for NoC-based MoT. This offer a new mapping algorithm based on discrete PSO for mapping cores of the graph to the routers. The results have been compared with the number of applications. This strategy has attained superior results within a reasonable period of time compared to the existing procedures.

2.16. Core Mapping to the Noc in Digital Circuit Design by Using Tabu Search method

In [16], the NoC structure is considered with a mesh topology, a new method for mapping the No Ccore has been introduced using a Tabu search (TS) algorithm. Operations of the gradual evolution in the genetic algorithms have been added to the TS processing in order to facilitate the computational efficiency. Laboratory results indicate that the core mapping needs time to obtain a value less than the conventional genetic algorithm according to the proposed method in this article.

2.17. Multi-Application Mapping Algorithm with Knowledge of the Reliability in the Noc

In [17], a mapping method with knowledge of reliability is recommended for multiple applications in the NoC. This method consists of three main steps [18]:

- A new core graph is developed through spares based on an applied core graph;
- To find the smallest rectangular area for installing applications given by using a heuristic algorithm;
- To search a specified area to the entire NoC and to select an area that will result in a minimum overall efficiency and energy consumption. Additional cores have been connected to all the applied core graph vertices and their edges have been weighted through the probability of fault of processing cores allocated to the application and they will be updated during the mapping process. A lot of the applied core graphs have been used to evaluate the proposed method. Results of 100,000 tests of fault injection show the decreased communicative energy and the improved efficiency in comparison with dependent methods known for both models of no errors and incomplete.

2.18. Runtime Mapping based on Applications Pre-Processing in NoC-based MPSoCs

In [19], the runtime heuristic method is proposed that smartly distributes applied tasks among multiple processors that consider communication overhead, computational load and operation of the source.

2.19. A Multi-Objective Adaptive Immune Algorithm for Multi- Application Noc Mapping

In [20], the use of multi-objective adaptive resistant algorithm (M^2AIA) has been proposed, an evolutionary approach for solving multi- application NoC mapping problem, delay and power consumption as multi-objective functions with a certain aim. To compare the efficiency of the method, the results have been compared with genetic mapping algorithms, branch and bound. A total of 11 well-known benchmarks have been tested, which includes random and real-world applications, and combinations of more than eight applications on the same SoC. Experimental results show that M^2AIA averagely reduces power consumption and delay to 27.3 and 42.1% compared with the branch and bound method, and 29.3 and 36.1 on genetic method.

2.20. Low- Energy Multi- Application Mapping Algorithm of Error Tolerance Capability in Noc-Based Multi-Processors

In [21], a multi-applicationmapping with error tolerance in the NoC-based multi-processor

substrates is offered. The proposed mapping method consists of two main components as follows:

- The mapping of an applied core graphic of processing cores without defect allowed;
- Putting the additional cores in the midst of other processing cores without independent defect. The first is a heuristic algorithm to put an applied core graph on the mapping substrate in order to achieve higher efficiency and a lesser communicative energy than previous methods. The next component adjusts position of additional cores on any application core graphics with regard to transient and steady-state core failures. With a suitable assignment of additional core, not only managing resources are well done, but also bounded defect in the system will be improved. Many applied core graphs that have been produced through TGFF, can be used to evaluate the proposed method. The results of experience of 1.000.000 fault injections show that at the 95% confidence level, the proposed method leads to the decreased communicative energy and the developed efficiency compared to the other methods.

2.21. Multi-Target Mapping Algorithm For No-cof E-mesh with a Specific Application

In [22], an optimization model for the mapping of the IP cores on a new NoC topology, E-mesh is recommended. As competition for a router port in E-mesh is hard, network competition, communication cost and also energy have been considered in this model. In order to solve the optimal model, a new multi- target mapping algorithm with a specific application has been presented on the intersection and jump of genetic algorithm-based E-mesh topology The experimental results show that, the proposed algorithm of the consumed energy, has less communication costs and network competition compared with the standard heuristic genetic algorithm.

3. Conclusion

In the research, first, the concept of mapping in NoC was briefly raised, then some of the mapping methods that use the evolutionary and the intelligent algorithms, such as genetics, the branches and bound, the bee colony, the ant colony, clustering, the structure of the tree, PSO, SA in the two-dimensional substrate, have been presented. In addition, important parameters for mapping NoC like power consumption, latency, congestion and communication costs for these algorithms has been evaluated. It should be noted that these methods can be used in the three-dimensional substrate as things that can be done in the future.

4. References

[1] Mohammad Fattah, Marco Ramirez, Masoud Daneshtalab (2012), Pasi Liljeberg, Juha Plosila, CoNA: Dynamic Application Mapping for Congestion Reduction in Many-Core Systems. In: Computer Design (ICCD), 2012 IEEE 30th International Conference on, 364–370, IEEE.

[2] L. Moller, L. S. Indrusiak, L. Ost, F. G. Moraes, and M. Glesner, (2012),Comparative analysis of dynamic task mapping heuristics in heterogeneous NoC-based MPSoCs, In Proceedings of the International Symposium on System on Chip (SoC),.

[3] Z. Deng , H. Gu , H. Feng , and B. Shu,(2011), Artificial Bee Colony Based Mapping for Application Specific Network-on-Chip Design, In Proceedings of the Second international conference on Advances in swarm intelligence (ICSI'11), Part I, PP. 285-292, Springer-Verlag Berlin, Heidelberg, ISBN: 978-3-642-21514-8.

[4] S. Tosun, (2011), New heuristic algorithm for energy aware application mapping and routing on mesh-based NoCs, In Proceedings of the Journal of System Architecture, Vol. 57, pp. 69–7.

[5] P. K. Sahu, N. Shah, K. Manna, and S. Chattopadhyay, (2011), A new application mapping strategy for mesh-of-tree based Network-on-Chip, In Proceedings of the IEEE International Conference on Emerging Trends in Electrical and Computer Technology (ICETECT), pp. 518–523.

[6] S. Tosun, (2011), Clustered-based application mapping method for Network-on-Chip, In Proceedings of the Journal of Advances in Engineering Software, Vol. 42, No. 10, pp. 868–874.

[7] P. K. Sahu, P. Venkatesh, S. Gollapalli, and S. Chattopadhyay (2011), Application mapping onto mesh structured Network-on-Chip using particle swarm optimization, In Proceedings of the IEEE International symposium on VLSI (ISVLSI), pp. 335–336.

[8] M. Zang and H. You,(2012), Low Power NOC Process Element Mapping Using Genetic Algorithm, In Proceedings of the Journal of Information and Computational Science, Vol. 9, No. 3, pp. 557–563.

[9] R. K. JENA,(2012) Application Mapping of Mesh based NoC Using Evolutionary Algorithm, In Proceedings of the Journal of Information Systems and Communication, Vol. 3, Issue 1, pp.-203-206, ISSN: 0976-8742 & E-ISSN: 0976-8750.

[10] B. Yang, L. Guang, T. Säntti, and J. Plosila,(2012), Parameter-Optimized Simulated Annealing for Application Mapping on Networks-on-Chip, In Proceedings of the 6th international conference on Learning and Intelligent Optimization (LION'12), pp. 307-322, Springer-Verlag Berlin,.

[11] B. Yang, L. Guang, T. Säntti, and J. Plosila,(2012), Tree-Model Based Contention-Aware Task Mapping on Many-Core Networks-on-Chip, In Proceedings of the Communications in Information Science and Management Engineering (CISME), Vol. 1, No. 6.

[12] M. Palesi, R. Tornero, J. M. Ordu˜na, V. Catania, and D. Panno,(2012), Designing Robust Routing Algorithms and Mapping Cores in Networks-on-Chip: A Multi-objective Evolutionary-based Approach, In Proceedings of the Journal of Universal Computer Science, vol. 18, no. 7, pp. 937-969.
[13] Q. Le, G. Yang, W. N. N. Hung, W. Guo,(2012), Reliable NoC Mapping Based on Scatter Search, In Proceedings of the Third international conference on Information Computing and Applications, ICICA (LNCS) , Vol. 7473, pp. 640-647,.
[14] Q. Le, G. Yang, W. N. N. Hung, X. Zhang, and F. Fan,(2013), A multi objective scatter search algorithm for fault-tolerant NoC mapping optimization, International Journal of Electronics.
[15] P. K. Sahu, A. Sharma, and S. Chattopadhyay, (2012), Application Mapping Onto Mesh-of-Tree Based Network-on-Chip Using Discrete Particle Swarm Optimization, In Proceedings of the 2012 International Symposium on Electronic System Design (ISED), pp. 172– 176.
[16] Z. Pan, and L. (2013)Chen, Mapping Cores to Network-on-Chip in Digital Circuit Design by Using Tabu Search Approach, In Proceedings of the Lecture Notes in Electrical Engineering, Vol. 3, pp 41-47.
[17] F. Khalili, and H. R. Zarandi, (2013) A Reliability-Aware Multi-application Mapping Technique in Networks-on-Chip, In Proceedings of the 21st Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), pp. 478-485.
[18] J. Wang, Y. Li, S. Chai, and Q. Peng,(2011) Bandwidth-aware application mapping for NoC-based MPSoCs, In Proceedings of the Journal of Computational Information Systems, Vol. 7, No. 1, pp. 152–159.
[19] S. Kaushik, A. Kumar Singh, (2011) and T. Srikanthan, Preprocessing-based Run-time Mapping of Applications on NoC-based MPSoCs, In Proceedings of the IEEE Computer Society Annual Symposium on VLSI, pp. 337-8.
[20] M. J. Sepu´lveda, W.J. Chau, G. Gogniat, and M. Strum,(2012), A multi-objective adaptive immune algorithm for multi-application NoC mapping, In Proceedings of the Analog Integrated Circuits and Signal Processing, Springer US, Vol. 73, No. 3, pp. 851–860.
[21] F. Khalili, and H. R. Zarandi,(2012), A Fault-Tolerant Low-Energy Multi-Application Mapping onto NoC-based Multiprocessors, In Proceedings of the IEEE Computer Society, 15th International Conference on Computational Science and Engineering (CSE), pp. 421-428.
[22] B. Zhang, H. Gu, S. Tian, and B. Li, (2012), A Multi-objective Mapping Strategy for Application Specific Emesh Network-on-Chip (NoC), In Proceedings of the ICSI, Vol. 7331, pp. 528-536.

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